METHOD OF IMPLEMENTATION - CABLE JITTER

Abstract

This test checks the amount of jitter added from an electrical cable and connector using the WAVECREST SIA 3000 and a pattern generator. This test is defined for a single lane and must be repeated for each lane of the DUT.

Coverage:

V2c07-016

Topology

(1X cable port) PhysicalCable1: Test_Fixture=LC1X_sma_L1, Width=1X

(4X cable port) PhysicalCable1: Test_Fixture=LC4X_sma_L2, Width=4X

(12X cable port) PhysicalCable1: Test_Fixture=LC12X_sma_L3, Width=12X

Two test fixtures are used at each end of the cable.

Qualifier   None

Notes

1. This test applies to both the cable and cable connector.
2. Test must be performed on each lane in the cable assembly.
3. A crosstalk source may be connected to either side of IB connection under test. Cross talk can be generated by a $1.6V_{pp}$ signal transmitted asynchrounously to the test pattern.
4. Total Jitter is defined as the pk-pk value at the data crossing point. The histogram must contain >10,000 hits for sufficient statistics.
5. Required instruments: SIA 3000 with A32 channel card option and Pattern Generator.

Dev Notes

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This test requires a cable test fixture. The proposal below is for 1X, 4X and 12X cables.
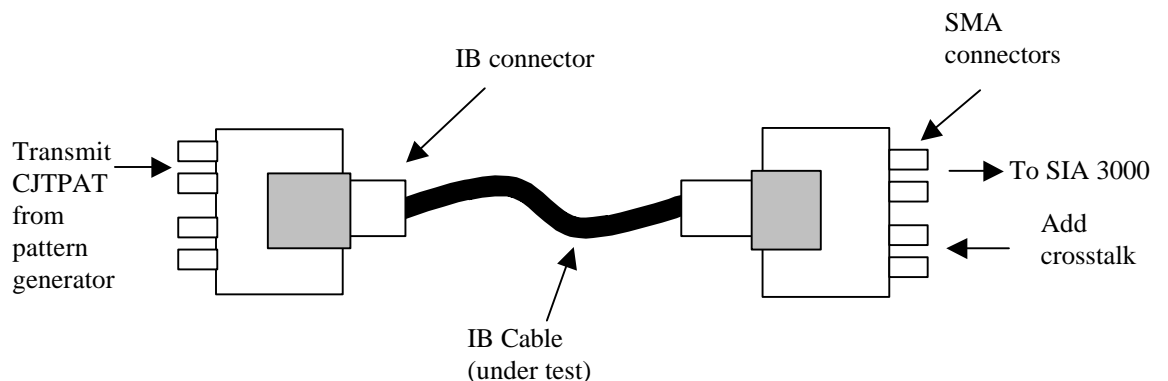
ALGORITHM

Assertions

V2c07-016#05

Initialization

1. Connect Pattern Generator differential pair to test fixture. Select CJTPAT as the test pattern for the pattern generator, Voltage level=1.6 Vpp, 2.5 Gb/s.
2. Connect SMA differential pair from test fixture output to channel input A of the SIA 3000.
3. For clock-to-data measurements connect the clock from the pattern generator to the channel input B of the SIA 3000.
4. Connect IB cable between IB connector-SMA adapter cards.

Tester Procedure

1. From the VISI Datacom window select the Random data with bitclock tool.

2. Measure signal voltage by depressing the [button icon] button

3. Click [button icon] to obtain a histogram with >10,000 hits.

4. Verify TJ pk-pk<0.25 UI or 100 ps. The figure below shows data from a typical acquisiton.

5. Test must be performed on each lane of the DUT

6. To measure the effects of crosstalk on 1X, 4X and 12X cable assemblies transmit a 2^7-1PRBS pattern at >1.3 Gb/s on the adjacent pair and then verify TJ<0.25 UI.